**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**



Applicants: Hassan S. Hashemi and Kevin J. Cote
Serial No.: 09/878,815
Filed: June 11, 2001
Art Unit: 2811
Examiner: Costanzo, Patricia M.
TITLE: Structure And Method For Fabrication Of A Leadless Chip Carrier

**APPLICANT'S DECLARATION UNDER 37 C.F.R. § 1.131**

Assistant Commissioner for Patents
Washington, D.C. 20231-0001

Dear Assistant Commissioner:

I, Hassan S. Hashemi, declare as follows:

1. I am an inventor of the subject matter described and claimed in United States Patent Application Serial No. 09/878,815, filed June 11, 2001, entitled "Structure And Method For Fabrication Of A Leadless Chip Carrier"; the subject matter is disclosed and claimed in the above-referenced patent application. The present application is a continuation-in-part of, and claims priority from, pending application Serial No. 09/713,834, filed November 15, 2000, which is in turn a continuation of Serial No. 09/252,851, filed February 17, 1999 and issued as patent number 6,191,477.

2. I declare that I conceived and reduced to practice the invention of the subject matter of the above-referenced application in the United States, as defined by claims 1-55, prior to January 29, 1999.

3. To evidence conception and reduction to practice of the invention of the subject matter of the above-referenced application in the United States, the following attached documents are submitted as evidence:

A. A copy of page 24 of the document "Packaging Technology Development Program," dated September 1998, describing a development schedule associated with developing and testing my invention. (Exhibit A)

B. A copy of pages 1 and 3 of the document "Package Design Group Monthly Report," dated January 29, 1999, describing design, testing, and analysis efforts of my invention. (Exhibit B)

4. I declare that the "LGA-QNL PACKAGE DEVELOPMENT" described on page 24 of "Packaging Technology Development Program," dated September 1998, is directed to my invention.

5. I declare that I am the author of the document entitled "Package Design Group Monthly Report," dated January 29, 1999.

6. I declare that the "RF-LGA" design, testing, and analysis efforts described on pages 1 and 3 of "Package Design Group Monthly Report," dated January 29, 1999, are directed to my invention.

7. I declare that the "RF-LGA" design, testing, and analysis efforts described on pages 1 and 3 of "Package Design Group Monthly Report," dated January 29, 1999, were completed prior to January 29, 1999.

8. I declare that page 24 of "Packaging Technology Development Program" and pages 1 and 3 of "Package Design Group Monthly Report," attached hereto, evidence conception and reduction to practice of the invention of the subject matter of the above-referenced application in the United States prior to January 29, 1999.

9. Alternatively, page 24 of "Packaging Technology Development Program" and pages 1 and 3 of "Package Design Group Monthly Report," attached hereto, evidence conception of the invention prior to January 29, 1999 and I declare that I exercised due diligence in reducing the invention to practice by, at latest, February 17, 1999 which is the filing date of a parent application Serial No. 09/252,851 (which is in turn the parent of application Serial No. 09/713,834, filed November 15, 2000, from which the present application claims priority).

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine of imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-referenced patent application or any patent issuing thereon.

Nov. 22, 2002
Date

S. Hassan Hashemi
Hassan S. Hashemi

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
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| Art Unit: | 2811 |
| Examiner: | Costanzo, Patricia M. |
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**APPLICANT'S DECLARATION UNDER 37 C.F.R. § 1.131**

Assistant Commissioner for Patents
Washington, D.C. 20231-0001

Dear Assistant Commissioner:

I, Kevin J. Cote, declare as follows:

1. I am an inventor of the subject matter described and claimed in United States Patent Application Serial No. 09/878,815, filed June 11, 2001, entitled "Structure And Method For Fabrication Of A Leadless Chip Carrier"; the subject matter is disclosed and claimed in the above-referenced patent application. The present application is a continuation-in-part of, and claims priority from, pending application Serial No. 09/713,834, filed November 15, 2000, which is in turn a continuation of Serial No. 09/252,851, filed February 17, 1999 and issued as patent number 6,191,477.

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11/22/02
Date

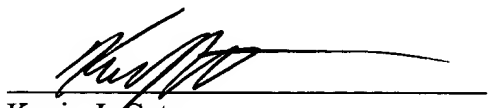
Kevin J. Cote

**EXHIBIT A**

## LGA - QNL PACKAGE DEVELOPMENT

| Project | NPEV | Resources |
|---|---|---|
| LGA - QNL PACKAGE DEVELOPMENT | | |

Description

Qualify new family of LGA-QNL laminate grid array packages for low to mid-lead count high performance applications.
Identify product(s), design & procure substrate, qualify vendors, assemble on MCM-L overmold and saw line, test, conduct failure analysis, and report

| Deliverables | Forecast | Actual |
|---|---|---|
| Identify lead product and line up support to qualify the package | 10/98 | |
| Design and get substrates from qualified suppliers – assemble parts | 12/98 | |
| Perform qualification testing, conduct failure analysis and write final report | 4/99 | |

**EXHIBIT B**

CONEXANT™

Date: Jan 29, 1999

**To:** Joe Adam
**From:** Hassan Hashemi
**Re:** Package Design Group Monthly Report

## Highlights:

A broad patent application is prepared on Low-Cost High Performance Multichip Module Design and Structure and will be filed prior to the press release on the MCMs. Four new MCMs and one RF-LGA™s were designed and submitted for procurement. The experimental test on using heat pipes to cool PA-MCM in a cell phone application was completed showing ~30 % decrease in junction temperature rise of a PA. A micro heat pipe is used to transfer the heat from the bottom surface of the PA- MCM to the cell phone antenna through a mixed convection - radiation mechanism. This breakthrough is similar to having Pentiurm processors in laptop computers allowing the use of powerful MCMs, e.g. PAs with >=3/8 duty cycle.

An invention disclosure was filed for a leadframe-LGA (LF-LGA™) which is similar to Amkor microleadframe (MLP) package suitable for low pin count RF and IF devices. This could be a lower package cost than substrate based LGAs, but all development work is on hold due to resource constraints. SD-NAD has identified ~20 products that will require some level of packaging support during the '99 calendar year, ranging from simple lead frame selections to complex multi-die BGA layouts. There is NOT sufficient resource to cover this.

MXL BGA assembly fails JEDEC level 3 qualification testing. Moisture sensitivity leading to popcorning is the primary issue. It is also recommend that additional testing be performed on 80um WB pitch in BGA devices since the material set and wirebond parameters are not the same as TQFP's.
The group MSPs are completed. Numerous performance enhancement, yield and quality improvement opportunities, and better communication of package / process design practices are identified that will be worked as a lead to the 2-year out technologies like Flip Chip and Wafer-level CSPs.

## 1. MCM & LGA Design & Analysis

**RM008** - Completed a new layout. This design has a single die DCS/GSM vs. a split die of DCS and GSM in the earlier design. All design guidelines were met. It was released to Toppan for an order of 2500 units on 1/25/99 for a quick turn. Design related documents were released on DMS.
**RM009** - Released design documents to DMS ( TW04-D275-003 & TW04-D275-005). -005 design was released to Toppan to build 1020 units. Both RM009D11-41 and RM009D11-51 were modified accordingly to identify the critical bond wire lengths and angles for both DCS and GSM outputs. Bond wire lengths were specified and they are to be within +/- 2 mils to achieve best electrical performance.
**RM907** – This single-band AMPS PA-MCM design was modified from a metal lid design to an overmolded one. The only change is that conductor ring is now covered with solder mask. One component pad to bond pad spacing currently stands at 12 mils (design rule stretch). Design was released to Toppan to build 1500 units on 1/20/99 with quick turn around.
**RM908** – This dual band PCS/AMPS design was released to Toppan to build 360 units with quick turn. 150 units are expected to be shipped to Nokia 3/4/99.
**RM909** – Obtained quotations from JVC and Ibiden on this 15x15 mm 4L uVia MCM. Still waiting for a response from Samsung and Hitachi. Initial quotes are at $1.50 – $2.30/unit at >=301kp/mo with 6-8 weeks delivery time!
**RM913** – This 6 x 6 mm PCS band PA MCM was laid out using the RM906 design for an overmolded process. In order to fit everything on this substrate, one component (C9) was removed from the new schematic. Currently, the design has not met 18 mils clearance between bond pads and component as spec (it is at 15 mils).
**RM801 PA/AMPS TDMA** - Released RM801 bonding diagram to DMS as requested by Farm and Mike Elbaz. Its PWB is the same as RM907, TW04-D385.

**Chip Array (0.8mm pitch) Qualification** – The qual work started on 1/28 after test board debug.

**RF-LGA solder joint reliability** – A parametric, 2-D axisymmetric DOE was developed to analyze the solder joint reliability of the RF-LGA package family. The FE model predicts relatively low plastic strain levels (0.5 – 0.9%) for all design considerations examined. Therefore, the existing pad solder joint design should provide sufficient reliability. Some design recommendations are as follows:

1. Proximity of solder joint edge to die edge should be at least 1mm for substrate thicknesses of 0.36mm. Thinner substrates will require a larger edge-to-edge distance and a larger solder joint length.
2. Pad solder joint size should be at least 0.35mm L x 0.30mm W.
3. The diameter of the center solder joint interconnection should be at least 60% of the package size.

**3.5mmx4.0mm RF-LGA for PAs** – This package was examined for solder joint reliability issues due to relatively low center pad to package ratio requirements. FE results predict plastic strain levels around 0.8%, which should yield a minimum of 500, -45C to 125C temperature cycles.

## 5. PRODUCTS DESIGNS & Qualifications

**Sabine – DID** Sabine was removed from the gated project list due to success in first silicon before the holiday shutdown. Cost of goods will determine ultimate success of this program. The BGA substrate, at $5, is seen as too costly. The product team is experimenting with a 2 layer BGA design from Amkor. If this trial demonstrates adequate performance, then the device will be converted to the 2 layer design. At that point, the SD Chip Carrier Layout group will modify the existing design to 2 layers for MXL production.

**Blackcomb/ Whistler - NAD ATM** Blackcomb-D/ Whistler substrates were received from Daisho. The Whistler design is scheduled to tape out by the end of January. Whistler will be used as the qual vehicle for 80 micron wirebond pitch in the BGA. Victor is nearing completion of the Whistler bond diagram.

**SuperPipe – DID** First pass silicon and substrate met expectations by the product group. Rev B silicon is currently in fab and is scheduled out by the first week of February. Production ramp is scheduled to begin in July. Qualification of the solid exposed gold die attach pad must be performed in SD.

**PMIC - WCD** PMIC 6x6 LGA qual devices were assembled in MXL prior to the holiday shutdown. Sockets should arrive in the 3rd or 4th week of February with an expected qualification completion date of 4/99.

**M46 and IA - WCD GSM** M46xx devices were assembled in Amkor's existing 160 CABGA. A modified design, adding a signal pin for more memory capability, is currently being fab'd by Amkor's substrate supplier. Substrates are due to the assembly factory on 2/27. M46xx devices will be assembled into this package for qualification and customer sampling. Expected volume for this device is 300K for FY99. A companion device will be packaged in the 10x10 CABGA with identical volumes for FY99.

**Wheezer - NAD T1/E1** Wheezer substrates were received from Daisho and 25 devices have been assembled in MXL for device debug. The remainder of the 500 pieces will be used for device qualification. This substrate design must be qualified since it is the first to use blind vias.

**Tornado - NAD ATM** Amkor is currently re-designing a 456 PBGA to add a power and ground plane. The package will also be used for a follow-on test chip (Countache II). Separate core and I/O power is routed in the new design.

**HDSL-2 - NAD DSL** NAD management has aggressive size requirements for the HDSL-2 BGA design. Customer expectations have been set on a 27mm body size. If not possible, a 31mm BGA may be acceptable. SD Chip Carrier Layout will perform trial layout of the 27mm design. If unsuccessful, the design will be given to Amkor as a 31mm package.